UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,091	07/22/2003	Takahiro Takemoto	NECA 20.522	8769

26304 7590 01/24/2007

KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
PHAM, TAMMY T	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,091	TAKEMOTO, TAKAHIRO	
	Examiner	Art Unit	
	Tammy Pham	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-11,13-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-11,13-16 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claims 2, 7, 12, 17 have been cancelled. Claims 1, 3-6, 8-11, 13-16, 18-24 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8-11, 13-16, 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over FURUYA (US Patent Application No: 2004/0104881 A1) in view of KIM et al. (US Patent No: 7,133,035 B2) and MORITA (US Application No: 2003/0011582 A1).

As for independent claims 1, 6, 11, 16, 21-24, FURUYA teaches of an active-matrix addressing LCD device (Fig. 3) and a method of driving an active-matrix addressing LCD device, comprising: a panel including an active-matrix substrate, an opposite substrate, and a liquid crystal layer sandwiched by the active-matrix substrate and the opposite substrate; the active-matrix substrate having data lines (Fig. 3, items D1-DK), scanning lines (Fig. 3, items G1-GM) that intersect with the data lines (Fig. 3, items D1-DK) at intersections, pixels (Fig. 3, items PIX) arranged near the respective intersections, and TFTs arranged as switching elements for the respective pixels (Fig. 3, item PIX); a source driver circuit (Fig. 3, item 5) for driving the data lines(Fig. 3, items D1-DK); a gate driver circuit (Fig. 3, item 7) for driving the scanning lines (Fig. 3, items G1-GM); and a controller circuit (not shown) for controlling the source driver

(Fig. 3, item 5) and the gate driver (Fig. 3, item 7); wherein the source driver (Fig. 3, item 5) has a resetting means (not shown) for resetting the data voltages outputted by the source driver circuit (Fig. 3, item 5) in a blanking period (Fig. 4, HORIZONTAL BLANKING PERIOD) of each of the horizontal synchronizing periods (Fig. 4) of the set (Fig. 4, item SIG) in section [0045].

FURUYA fails to teach that (1) a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is ***inverted in every set of two or more horizontal synchronizing periods*** by the controller circuit; and (2) wherein the resetting means performs its resetting operation ***with reference to a latch signal*** supplied to the source driver circuit by the controller circuit.

KIM teaches that a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is ***inverted in every set of two or more horizontal synchronizing periods*** by the controller circuit in Fig. 4 and in column 4, lines 59-61.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the alternating polarity of the data voltage in every set of two or more horizontal synchronizing period as taught by KIM with the active matrix of FURUYA because this is a well known method in driving a display and in inverting less often, one uses less power and hence creates a more power efficient model.

MORITA teaches that the resetting means performs its ***resetting operation with reference to a latch signal*** supplied to the source driver circuit by the controller circuit (Fig. 18, item 60) in section [0207].

It would have been obvious to one with ordinary skill in the art at the time the invention was made to utilize the signals from the controllers as taught by MORITA to implement the resetting means as taught by FURUYA and KIM because utilizing a known process in the art can help cut cost by expanding upon the known idea of a common controller that supplies various signals to the drivers of a display.

As for independent claims 6, 16, the claim limitations has been address in the rejection of independent claim 1 as stated above with the exception of the claim limitation in which FURYUYA fails to teach that the source driver has a polarity inverting means for inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of ***each of the horizontal synchronizing periods*** of the set.

KIM teaches that a polarity of a data voltage applied to each of the pixels by way of a corresponding one of the data lines and a corresponding one of the TFTs is ***inverted in every set of two or more horizontal synchronizing periods*** by the controller circuit in Fig. 6 and in column 4, lines 44-47.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the alternating polarity of the data voltage in every set of a horizontal synchronizing period as taught by KIM with the active matrix of FURUYA because this is a well known method in driving a display and in reversing the polarity more frequently, one reduces the amount of flickering.

As for independent claims 21, 23, the claim limitations has been address in the rejection of independent claim 1 as stated above with the exception of the claim limitation in which FURYUYA fails to teach that the ***source driver has a resetting means*** for resetting the data voltages outputted by the source driver in a blanking period of each of the horizontal periods of the set; and wherein the polarity of the data voltages supplied by way of the data lines is alternatively inverted in every set of the two horizontal synchronizing period and in every vertical synchronizing period within every frame period, thereby driving the device by a ***2-H dot inversion method***.

MORITA teaches that the ***source driver has a resetting means*** for resetting the data voltages outputted by the source driver in section [0207].

It would have been obvious to one with ordinary skill in the art at the time the invention was made to utilize the signals from the controllers as taught by MORITA to implement the resetting means as taught by FURUYA and KIM because utilizing a known process in the art can help cut cost by expanding upon the known idea of a common controller that supplies various signals to the drivers of a display.

KIM teaches that the polarity of the data voltages supplied by way of the data lines is alternatively inverted in every set of the two horizontal synchronizing period (Hsync) and in every vertical synchronizing period (Vsync) within every frame period, thereby driving the device by a 2-H dot inversion method in Figs. 3a-b and in column 3, lines 45-48 and in column 4, lines 13-17.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to implement the 2-H dot inversion method as taught by KIM with the display driving

devices of FURUYA because it is a way known method in driving an active matrix display device, which refreshes at a much faster rate than a passive matrix display.

As for independent claims 22, 24, the claim limitations has been address in the rejection of independent claims 1, 21 as stated above with the exception that FURUYA fails to teach that the source driver has a polarity inverting means.

KIM teaches that the source driver (not shown) has a polarity inverting means in Figs. 3a-b and in column 3, lines 45-48.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to implement the polarity inverting method as taught by KIM with the display driving devices of FURUYA because it is a way known method in driving an active matrix display device, which refreshes at a much faster rate than a passive matrix display.

As for claims 3, 8, 13, 18, FURUYA, KIM and MORITA fails to teach that each of the data voltages alternately has a positive value or a negative value in the polarity inversion period; and wherein the resetting means is controlled in such a way that each of the data voltages will ***reach a middle point value*** between the positive value and the negative value after the resetting operation is completed.

Examiner takes ***official notice*** that it is well known in the art to have each of the data voltages alternately has a positive value or a negative value in the polarity inversion period; and wherein the resetting means is controlled in such a way that each of the data voltages will ***reach***

a middle point value between the positive value and the negative value after the resetting operation is completed.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine specify that the resetting means enables the value of the voltage to reach a middle point in regards to both the negative and positive value.

As for claims 4, 9, 14, 19, KIM teaches that the polarity of the data voltages (POL1) supplied by way of the data lines is alternately inverted in every set of the two horizontal synchronizing periods and in every vertical synchronizing period within every frame period, thereby driving the device by a 2-H dot inversion method in column 4, lines 13-17.

As for claims 5, 10, 15, 20 KIM teaches that the polarity of the data voltages (POL2) supplied by way of the data lines is alternately inverted in every set of the two horizontal synchronizing periods (Hsync) within every frame period, thereby driving the device by a 2-H line inversion method in Fig. 6 and in column 4, lines 59-62.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-6, 8-11, 13-16, 18-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
January 20, 2007

Tammy Pham
Patent Examiner
Technology Division 2629

JIMMY NGUYEN
PRIMARY EXAMINER